

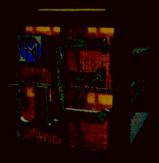
New Millennium Program Deep Space 1 Micro-Electronics Systems Technologies







Micro-Electronic Systems Integrated Product Development Team



The Team



Our Technologies



The Micro-Electronics Systems Integrated Product Development Team



National Aeronautics and Space Administration



Jet Propulsion Laboratory



Lewis Research Center





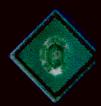
Air Force/ Phillips Laboratory



Hughes Telecommunications & Space



Lockheed Martin



Georgia Institute of Technology





Optivision Corporation



University of Southern California



Goddard Space Flight Center



Honeywell

IRVINE SENSORS CORP.

Irvine Sensors Corporation



Space Computer Corporation







Current Technologies

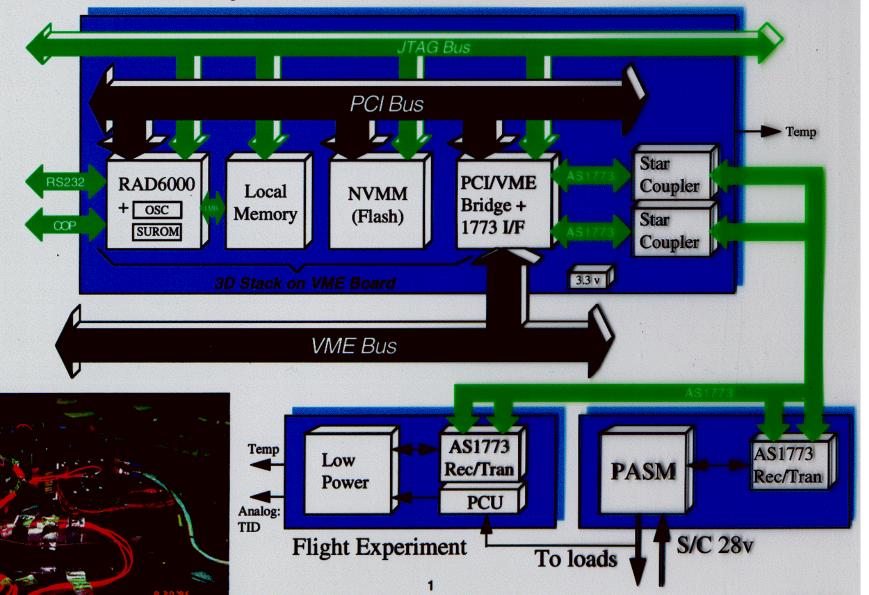
- 3D Stack Space Computer
- Mass Storage
- Low Power Electronics
- Power Actuation and Switching Module
- Distributed Reliable Computing



Example of the NMP/DS1 System Architecture



L. Alkalai 6/24/96



2-14





3-D Packaging

Capabilities

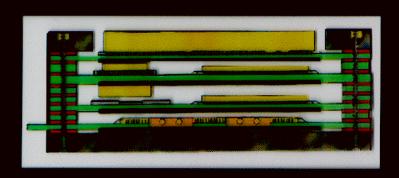
- Stack of 4 MCMs (Processor, Memory, 1 O, SSR)
- 5.8" x 4.0" x 2.1"
- 360 I/O Pads @ 32-mil Pitch
- MCM Bonded to Substrate Holders. Substrate Holders Stacked and Connected by Elastomeric Elements
- Re-workable Without Special Process
- Design for Testability with Boundary Scan

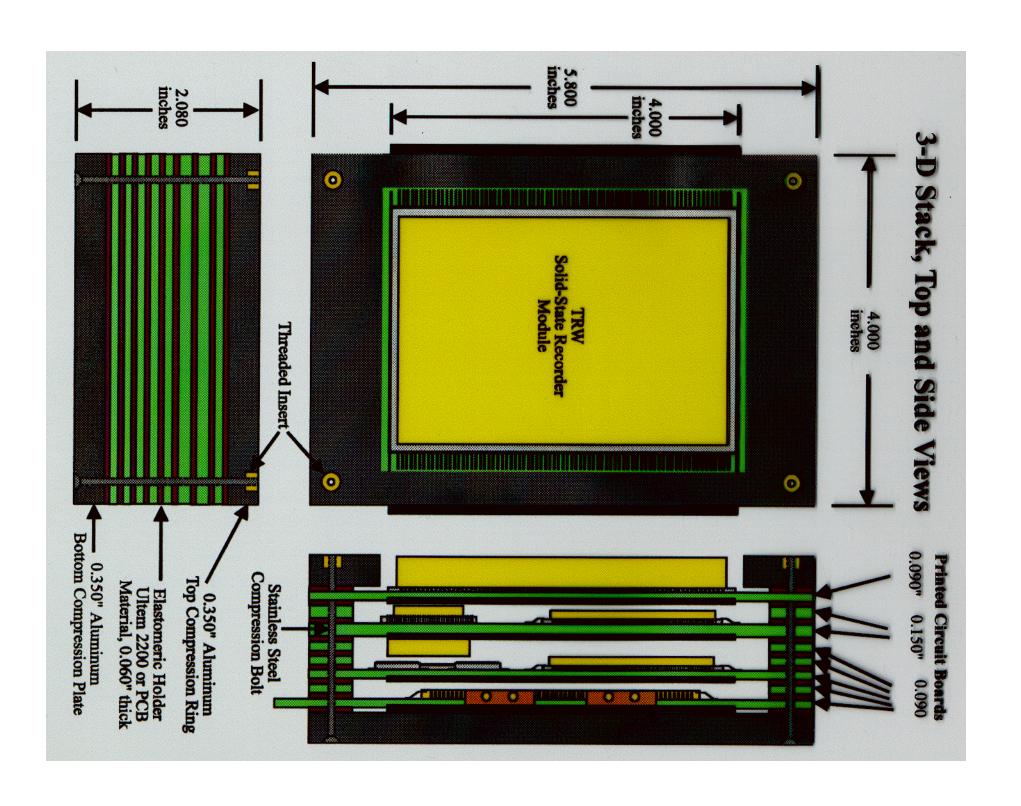
Partnership

Space Computer Corporation

Benefits

Step Toward Direct MCM Stacking



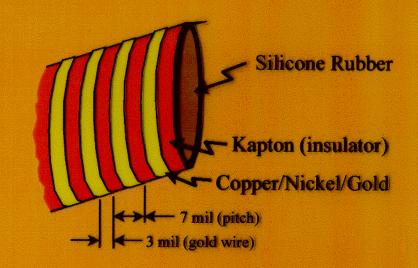


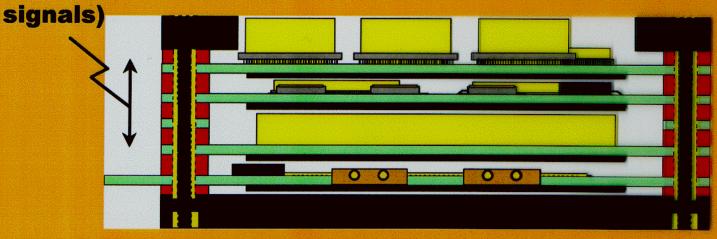
Microelectronics 3D Stack

Elastomeric Interconnect

The elastomer provides a highly dense interconnection mechanism between "slices" in the stack

Each interconnect side of the stack has 156 signals (312 total interconnect

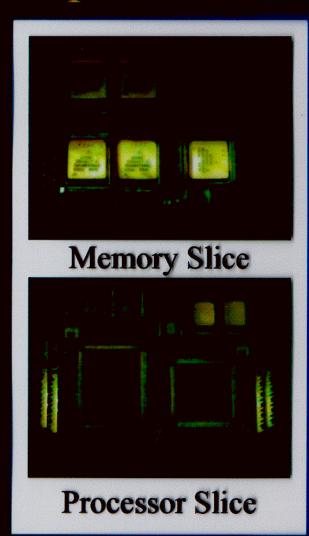






3D Stack Space Computer

- 5.8" x 4.0" x 2.1" Form Factor
- 3 Dimensional Stacking of Slices
- 33 MHz Rad-6000
 - 32 Bit RISC Processor
 - Commercial PCI Interface
 - Commercial OS: VxWorks
- 320 MB DRAM
 - 100x Reduction of Mass & Volume Relative to PCB
 Technology
- 1773 Interface
- Point of Contact: Dwight Geer, JPL





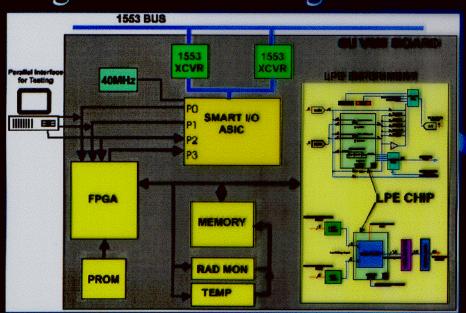
Mass Storage

- Non-Volatile Memory Modules
 - − 1 Gigabit Storage Per Slice
 - Can Have Multiple Slices
 - All Solid State, No Moving Parts
- Point of Contact: Dwight Geer, JPL





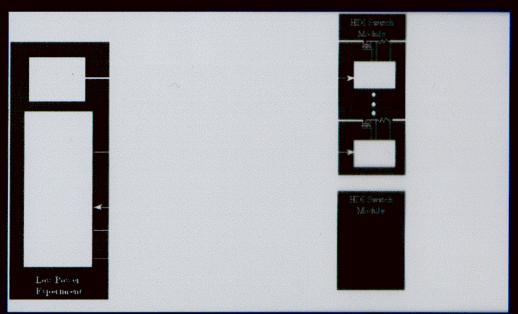
- .25 µm Silicon-on-Insulator CMOS
 - Extremely Low Power
 - Inherently Rad-hard
 - Capable of Extremely High Levels of Integration
 - 0.18 μm CMOS/SOI
 is being developed
- Point of Contact:
 - Eric Holmberg, JPL





Power Actuation and Switching Module

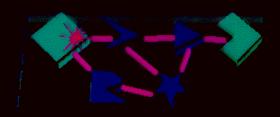
- High Voltage, Mixed Signal ASICs
- Uses HDI Technology
- 8 Power Switches Outputs
- Point of Contact: Greg Carr, JPL



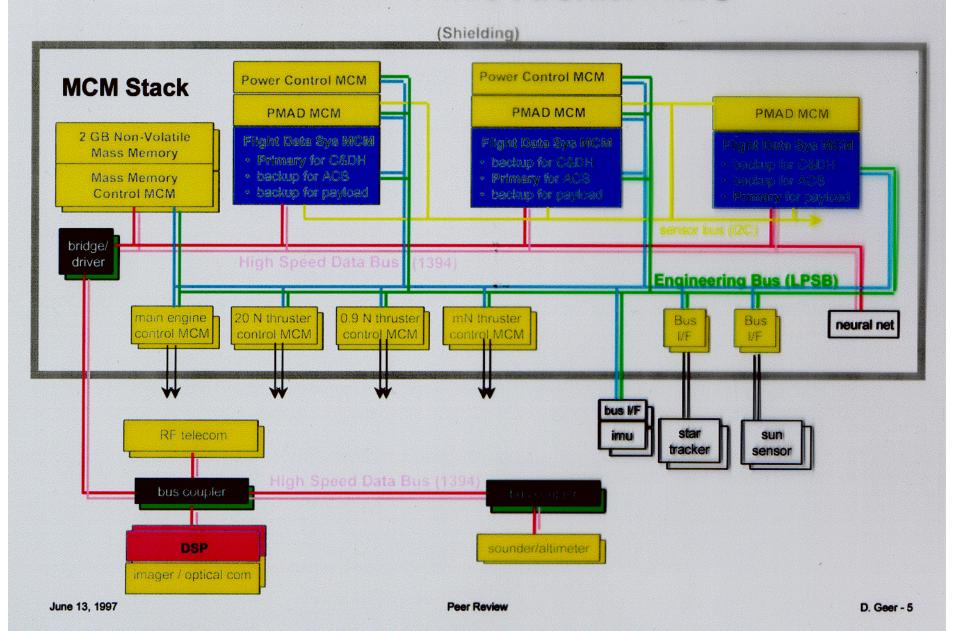


Distributed Reliable Computing

- Commercial Off The Shelf Hardware
- Asynchronous, Message Based Application Software
- Software Implemented Fault Tolerance Inserted Into Message Passing System
- Integrated I/O Architecture Significantly Reduces
 Software Complexity and Performance Requirements
- Heirarchical, Reliable Network/bus Architecture Supporting Standard Network Protocols
- Point of Contact: David Smythe, JPL



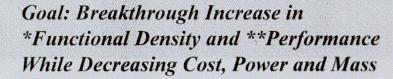
X2000 Avionics Architecture





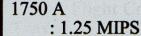
Evolution of Computers for Deep Space

**>2000XrFOM



**
$$rFOM = \frac{Delay \times Power}{Density}$$
Relative Figure of Merit at IC Level

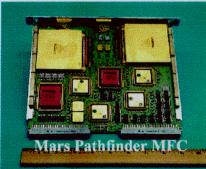
**20XrFOM



Functionality: *Command and Data Handling

**1XrFOM





RAD6000 RISC

2.5 to 22

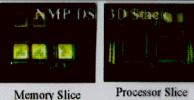
MIPS

Functionality: *Command and Data Handling

*Attitude Determination and Control

**117X.FOM



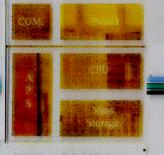


: RAD6000

RISC Flight Computer 2.5 to 55MIPS, very high perf. PCI and 1773 I/O, low power electronics

Functionality:

- *Command and Data Handling
- *Attitude Determination and Control
- *Mass Storage (nonvolatile)
- *Power Management & Distribution (PMAD)



100s of MIPS

Functionality:

- *Command and Data Handling
- *Attitude
- Determination and Control
- *Mass Storage
- *PMAD
- *Sensor electronics, mixed signal, DSP
- *Telecom
- *GN&C sensors and MEMS
- *Evolvable system
- *Reconfigurable
 Hardware
- *Major use of IP